Notice of Allowability	Application No.	Applicant(s)	
	09/757,798	BOLTON, JERRY THOMAS	
	Examiner	Art Unit	
	YOUNG T. TSE	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed 18 January 2005*.

2. ☒ The allowed claim(s) is/are *1-23*.

3. ☒ The drawings filed on *16 April 2002 and 21 July 2004* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Ross R. Viguet on March 07, 2005.

The application has been amended as follows:

In the Specification:

On page 17, line 25, "one LSB" has been changed to "one least significant bit (LSB)" to define LSB as recited in the amended claims 1, 15 and 20.

In the Claims:

In claim 1, line 7, "reference signal" has been changed to "reference signal by at least one least significant bit".

In claim 15, line 11, "reference" has been changed to "reference by at least one least significant bit".

In claim 20, line 8 and line 9, "selected of" and "reference signal" have been changed to "selected ones of" and "reference signal by at least one least significant bit", respectively.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YOUNG T. TSE whose telephone number is (571) 272-3051. The examiner can normally be reached on Monday and Wednesday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YOUNG T. TSE
Primary Examiner
Art Unit 2637

DETAILED DESCRIPTION

A preferred embodiment of the present invention enhances the noise characteristics of multi-order delta-sigma modulators by preferably including a quantizer in every modulator stage after the first, which may be selectively programmed to vary the reference signal associated therewith. To achieve the improved response, the preferred embodiment of the present invention would vary the subsequent stages' reference signals to be different from the first stage reference signal.

FIGURE 6 shows a preferred embodiment of the present invention configured as a digital MASH second-order delta-sigma modulator. The inventive system generally receives input signal 6000 into stage one modulator 61. Input signal 6000 typically passes through stage one summer 610 which subtracts stage one output signal 6013 to form stage one intermediate signal 6011. Stage one intermediate signal 6011 is then usually integrated by integrator 611 to form stage one integrated signal 6012, which is then typically quantized by quantizer 612 using reference signal 6110. Quantizer 612 then usually outputs stage one output signal 6013 to output summer 600. Stage one output signal 6013 also typically feeds back to stage one summer 610 for subtracting from input signal 6000 to form stage one intermediate signal 6011.

Because of its MASH configuration, the negative of stage one output signal 6013 is also usually fed to summer 615 to be subtracted from integrated signal 6012. The resulting stage one quantization error signal is then typically fed forward into stage two modulator 62. In the second stage, this stage one quantization error signal 6014 typically passes through stage two summer 620 wherein stage two output signal 6023 is subtracted. The resulting stage two intermediate signal 6021 is then integrated by integrator 621 to form stage two integrated signal 6022, which is then quantized by quantizer 622 preferably using reference signal 6120. According to the preferred embodiment of the present invention, reference signal 6120 preferably differs from reference signal 6110 by one least significant bit (LSB). Quantizer 622 usually outputs stage two output signal 6023 to the output summer 600 to be added to stage one output signal 6013 to form modulated output signal 6001. A digital differentiator 623 is placed between quantizer 622 and output summer 600 which shapes the noise within stage

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A multi-staged delta-sigma modulator comprising:

a first delta-sigma modulator of a first stage having a first quantizer input reference signal;

at least one subsequent delta-sigma modulator of at least one subsequent stage cascaded from said first stage, each of said at least one subsequent delta-sigma modulator having a quantizer input reference signal variable in relation to said first quantizer input reference signal by at least one least significant bit; and

a set of differentiators disposed in each of said at least one subsequent stage, an input of said set of differentiators in communication with an output of each of said at least one subsequent stage.

2. (Previously Presented) The modulator of claim 1 further comprising a final adder for summing outputs of said first stage and an output of each of said set of differentiators.

~~3.~~ 4. (Original) The modulator of claim 1 wherein an input to said multi-staged delta-sigma modulator is a digital signal.

~~4.~~ 5. (Currently Amended) The modulator of claim ~~3~~ 4 wherein said set of differentiators comprises a number of digital differentiators equal to a number of said stages before said subsequent stage on which said set of differentiators is disposed.

~~5.~~ 6. (Original) The modulator of claim 1 wherein said at least one subsequent delta-sigma modulator comprises two or more subsequent delta-sigma modulators.

~~6.~~ 7. (Currently Amended) The modulator of claim ~~5~~ 6 wherein each of said quantizer input reference signals of said two or more subsequent modulators is different from another of said quantizer input reference signals.

12
7. (Currently Amended) ~~The modulator of claim 5~~ A multi-staged delta-sigma modulator comprising:

a first delta-sigma modulator of a first stage having a first reference signal;

at least one subsequent delta-sigma modulator of at least one subsequent stage cascaded from said first stage, each of said at least one subsequent delta-sigma modulator having a reference signal variable in relation to said first reference signal, wherein said at least one subsequent delta-sigma modulator comprises two or more subsequent delta-sigma modulators, wherein each of said reference signals of said two or more subsequent modulators is substantially equal to another of said reference signals and wherein said substantially equal reference signals are different from said first reference signal; and

a set of differentiators disposed in each of said at least one subsequent stage, an input of said set in communication with an output of each of said at least one subsequent stage.

13
8. (Currently Amended) ~~The modulator of claim 5~~ A multi-staged delta-sigma modulator comprising:

a first delta-sigma modulator of a first stage having a first reference signal;

at least one subsequent delta-sigma modulator of at least one subsequent stage cascaded from said first stage, each of said at least one subsequent delta-sigma modulator having a reference signal variable in relation to said first reference signal, wherein said at least one subsequent delta-sigma modulator comprises two or more subsequent delta-sigma modulators, wherein at least two of said reference signals of said two or more subsequent modulators are substantially equal to another of said reference signals and wherein said substantially equal reference signals are different from said first reference signal; and

a set of differentiators disposed in each of said at least one subsequent stage, an input of said set in communication with an output of each of said at least one subsequent stage.

14 13
9. (Original) The modulator of claim ~~8~~ wherein said reference signals of a remainder of said two or more subsequent delta-sigma modulators are substantially equal to said first reference signal.

8
10. (Original) The modulator of claim 1 wherein said first delta-sigma modulator comprises a multi-stage delta-sigma modulator.

9
~~11.~~ (Original) The modulator of claim 1 wherein at least one of said subsequent delta-sigma modulators comprises a multi-stage delta-sigma modulator.

10
~~12.~~ (Currently Amended) The ~~invention~~ modulator of claim 1 further comprising:

an interpolation filter prior to said first stage for increasing a sampling rate of ~~said~~ an input signal.

11
~~13.~~ (Previously Presented) The modulator of claim 1 wherein said modulator is constructed substantially on a single integrated circuit substrate.

3
~~14.~~ (Previously Presented) The modulator of claim 2 wherein said modulator is constructed substantially on a single integrated circuit substrate.

15. (Previously Presented) A method for modulating signals comprising the steps of:

producing a first modulated signal from an input signal in a first delta-sigma modulator stage using a first reference;

producing subsequent modulated signals in subsequent delta-sigma modulator stages using subsequent references;

differentiating said subsequent modulated signals;

adding said first modulated signal and said subsequent modulated signals into a final output; and

programming at least one of said subsequent references to be different from said first reference by at least one least significant bit.

16. (Currently Amended) The method of claim 15 wherein said producing said first modulated signal step comprises the steps of:

integrating ~~a revised~~ an intermediate input signal;

quantizing said integrated input signal using said first reference;

subtracting said quantized signal from said input signal to form said ~~revised~~ intermediate input signal;

outputting said quantized signal as said first modulated signal;

subtracting said first modulated signal from said integrated input signal to form a stage error signal; and

outputting said stage error signal for use in said producing said subsequent modulated signals step.

17. (Previously Presented) The method of claim 15 wherein said producing said subsequent modulated signals step comprises the steps of:

integrating a modified quantization error signal;

quantizing said integrated error signal using one of said subsequent references to produce a subsequent modulated signal;

subtracting said subsequent modulated signal from a prior stage error signal to produce said modified quantization error signal; and

outputting said subsequent modulated signal.

18. (Original) The method of claim 17 wherein said producing said subsequent modulated signal step of each of said subsequent modulated signals prior to a final subsequent modulated signal further comprises the steps of:

subtracting said subsequent modulated signal from said integrated error signal to form a subsequent stage error signal; and

outputting said subsequent stage error signal.

19. (Previously Presented) The method of claim 15 further comprising the step of:

increasing a sampling rate of said input signal prior to said step of producing said first modulated signal.

20. (Currently Amended) A system for modulating signals using a multi-order delta-sigma modulator comprising:

means for receiving an input signal to be modulated;

means for producing a first intermediate modulated signal with a first delta-sigma modulator stage within said multi-order delta-sigma modulator using a first reference signal;

means for producing subsequent intermediate modulated signals with one or more subsequent delta-sigma modulator stages within said multi-order delta-sigma modulator using subsequent reference signals, wherein selected ones of said subsequent reference signals are selectively variable in relation to said first reference signal by at least one least significant bit; and

means for summing said first intermediate modulated signal with said subsequent intermediate modulated signals to produce a modulated output signal~~; and~~

~~means for providing said modulated output signal to an output of said multi-order delta-sigma modulator~~.

21. (Original) The system of claim 20 further comprising:

means for differentiating said subsequent intermediate modulated signals.

22. (Previously Presented) The system of claim 20 further comprising:

means for increasing a sampling rate of said input signal prior to said means for producing said first intermediate modulated signal.

23. (Original) The system of claim 20 wherein said subsequent reference signals are each different from said first reference signal.